What is claimed is:

1. A semiconductor memory comprising:

a core array including a plurality of memory cells;

a redundant array to be substituted for a substitution object area including a defective cell in the core array;

a substitution address memory storing an address of a first substitution object area including both sides of the defective cell as a substitution object address; and

a redundancy controller controlling to substitute the redundant array for the core array,

wherein, when the first substitution object area is entirely located on the inside of the core array, said redundancy controller controls to substitute the redundant array for said first substitution object area corresponding to the substitution object address, and when a portion of the first substitution object area is located on the outside of the core array, the redundancy controller controls to substitute the redundant array for a second substitution object area which includes the defective cell and is located on the inside of the core array, irrespective of the substitution object address.

2. The semiconductor memory according to claim 1,

wherein the redundancy controller compares an access address supplied at a time of access with the substitution object address, and the first substitution object area is replaced by the redundant array according to the comparison

result.

3. The semiconductor memory according to claim 1, wherein the core array comprises a plurality of blocks, and the substitution object address includes a block address and an in-block address, and

when the first substitution object area extends to the neighboring blocks, the redundancy controller substitutes the redundant array for either one of the neighboring blocks, depending on the comparison result between an access address supplied at a time of access and the in-block address.

4. The semiconductor memory according to claim 1, wherein the core array comprises a plurality of blocks and each of the plurality of blocks comprises a plurality of sub-blocks, and the substitution object address includes a block address, a sub-block address and an address in the sub-block, and

when the first substitution object area extends to the neighboring sub-blocks, the redundancy controller substitutes the redundant array for either one of the blocks of the neighboring sub-blocks, depending on the comparison result between an access address and the address in the sub-block.

5. A semiconductor memory comprising:

a core array including a plurality of blocks each having a plurality of memory cells;

a redundant array to be substituted for a substitution object area including a defective cell in the core array;

a substitution address memory storing an address of a first substitution object area including both sides of the defective cell as a substitution object address; and

a redundancy controller controlling to substitute the redundant array for the core array depending on said substitution object address,

wherein, when the first substitution object area is entirely located on the inside of the core array, and extends to both neighboring blocks, the redundancy controller selects either one of said neighboring blocks depending on an access address so as to substitute the redundant array for said selected block, and

when a portion of the first substitution object area is located on the outside of the core array, the redundancy controller controls to substitute the redundant array for a second substitution object area which includes the defective cell and is located on the inside of the core array.

6. The semiconductor memory according to claim 5,

wherein the redundant array is of the same size as each block,

the substitution object address includes a block

address and an in-block address of the block which are indicative of the first substitution object area, and

the redundancy controller selects either one of the neighboring blocks by comparing the access address with the in-block address.

7. The semiconductor memory according to claim 5,

wherein each block in the core array further comprises a plurality of sub-blocks,

the redundant array is of the same size as each sub-block,

the substitution object address includes a block address, a sub-block address of the sub-block, and an address in the sub-block of the block which are indicative of the first substitution object area, and

the redundancy controller selects either one of the neighboring blocks by comparing the access address with the address in the sub-block.

8. The semiconductor memory according to claim 7,

wherein when the first substitution object area extends to the neighboring sub-blocks, the redundancy controller selects either one of said neighboring sub-blocks depending on the access address, and controls to substitute the redundant array for said selected sub-block.

9. The semiconductor memory according to claim 5,

wherein each of the plurality of blocks is provided corresponding to each output terminal, and

when the first substitution object area is entirely located on the inside of the core array and extends to both neighboring blocks, the redundancy controller controls to substitute an output of the redundant array for an output of either one of the neighboring blocks depending on the access address, and

when a portion of the first substitution object area is located on the outside of the core array, the redundancy controller controls to substitute the output of the redundant array for an output of the second substitution object area.

10. The semiconductor memory according to claim 5,

wherein the memory cell comprises a cell transistor having a trap gate for storing charge, and the neighboring cell transistors are connected to a common bit line.

11. The semiconductor memory according to claim 5 further comprising a reference array sandwiched between the blocks,

wherein when a portion of the first substitution object area is located in the reference array positioned on the outside of the core array, the redundancy controller controls to substitute the redundant array for the second

substitution object area.

12. The semiconductor memory according to claim 5, wherein the substitution object address includes a start address of the first substitution object area, and when the first substitution object area includes an outer address than the uppermost address of the core array, the redundancy controller controls to substitute the redundant array for the second substitution object area.

13. The semiconductor memory according to claim 5, wherein the substitution object address includes an end address of the first substitution object area, and when the first substitution object area includes an outer address than the lowermost address of the core array, the redundancy controller controls to substitute the redundant array for the second substitution object area.